

Analysis and Simulation of Seven Level Inverter System

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Abstract

This paper deals with the analysis and simulation of the seven level inverter. This paper presents the seven level inverter with harmonics reduction along with the reduction. The percentage (%) total harmonic distortion is calculated for seven level inverter. The harmonic reduction is achieved by selecting appropriate switching angles. The functionality verification of the seven level inverter is done using MATLAB.

Key words: Neutral point clamped inverter, cascaded multi level inverter.

I. INTRODUCTION

The multi level inverter was first introduced in 1975. The three level converters was the first multi level inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is their small output voltage, results in higher output quality, lower harmonic component, better electro magnetic computability, and lower switching losses. [2]

Multilevel inverter include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less switching frequency, higher efficiency, lower voltage devices and better electromagnetic compatibility[4]. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltages at the output, while the power semiconductors must withstand only reduced voltage.

II. (a). H – BRIDGE INVERTER

Another characteristic is that the “H” topology has many redundant combinations of switches’ positions to produce the same voltage levels. As an example, the level “zero” can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on [7] [8] [9]. Another characteristic of “H” converters is that they only produce an odd number of levels, which ensures the existence of the “0V” level at the load .For example, a 51-level inverter using an “H” configuration with transistor-clamped topology requires 52 transistors, but only 25 power supplies instead of the 50 required when using a single leg [8]. Therefore, the problem related to increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50%.

Figure.1.a shows the single-phase H – Bridge of cascaded inverter. The ac terminal voltages of each bridge are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage balancing capacitors. This configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters, and reactive power compensation.

In this case, the power supply could also be voltage regulated dc capacitor. The circuit diagram consists of two cascade bridges. The load is connected in such a way that the sum of output of these bridges will appear across it. The ratio of the power supplies between the auxiliary bridge

and the main bridge is 1:3. One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementation of these topologies. [9]

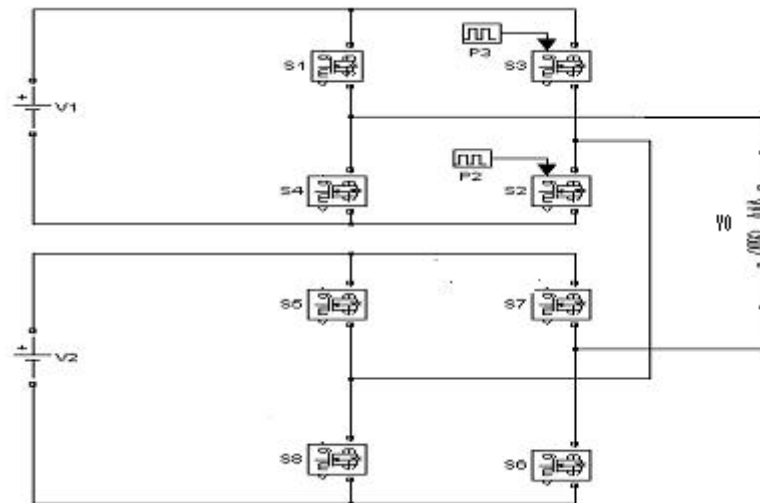


Fig . 1.a. H – Bridge Inverter

Table 1: Switching Sequence of H – Bridge Inverter

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8
-4Vdc	0	0	1	1	0	0	1	1
-3Vdc	0	0	1	1	0	0	0	0
-2Vdc	0	0	1	1	1	1	0	0
-1Vdc	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0
+1Vdc	0	0	0	0	1	1	0	0
+2Vdc	1	1	0	0	0	0	1	1
+3Vdc	1	1	0	0	0	0	0	0
+4Vdc	1	1	0	0	1	1	0	0

Using H-Bridge inverter the harmonics was reduced in 3 and 7 level output voltages. The inverter generates a high quality output voltage waveform. It reduces dv/dt stress imposed on power switching devices and also harmonic components of output voltage and load current quite well.

The phase output voltage is synthesized by the sum of two inverter outputs. Each inverter bridge is capable of generating three different levels of voltage outputs. The main bridge can generate +3Vdc, 0, -3Vdc and the auxiliary bridge can generate +Vdc, 0, -Vdc. By using appropriate combinations of switching devices many voltage levels are obtained. When the positive group switches are turned on the voltage across that particular bridge is positive. When the negative group switches are turned on the voltage across that particular bridge is negative. When S1, S2 are turned on the voltage across the main bridge is +3Vdc.

When S3, S4 are turned on the voltage across the main bridge is - 3Vdc. When S5, S6 are turned on the voltage across the auxiliary bridge is +Vdc. When S7, S8 are turned on the voltage across the auxiliary bridge is -Vdc. To obtain +2Vdc the switch combinations S1, S2, S7 & S8 are turned on. To obtain +4Vdc the switch combinations S1, S2, S5 & S6 are turned on. To obtain - 2Vdc the switch combinations S3, S4, S5 & S6 are turned on. To obtain -4Vdc the switch combinations S3, S4, S7 & S8 are turned on. The table.1 shows the switching strategy of

transistors at each level. The status of the switch is '0', that switch is in OFF condition. The status of the switch is '1', that switch is in ON condition.

(b). Harmonic Reduction:

To eliminate 5th, 7th, and 9th order harmonics, the firing angles for each level is found by solving the following equations.

$$\begin{aligned} \cos 5a_1 + \cos 5a_2 + \cos 5a_3 + \cos 5a_4 &= 0 \\ \cos 7a_1 + \cos 7a_2 + \cos 7a_3 + \cos 7a_4 &= 0 \\ \cos 9a_1 + \cos 9a_2 + \cos 9a_3 + \cos 9a_4 &= 0 \end{aligned}$$

Using Math CAD, the values of the "a" is obtained as follows

- a1 = 12.834
- a2 = 29.908
- a3 = 50.993
- a4 = 64.229

Where a1, a2, a3, a4 are the firing angles in degrees.

The switching pulses are obtained by carrying out the above calculation.

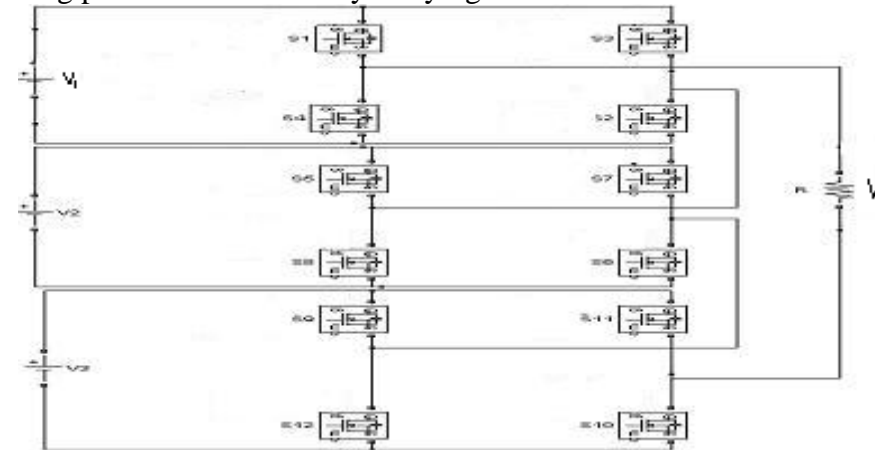


Fig. 2.a. H – Bridge 7 – Level Conventional Inverter

The H-Bridge 7-level conventional inverter is shown in the figure 2.a. The conventional 7- level inverter has some disadvantages they are requires 2(m-1) switching devices; increase the cost; large in size; controlling is complex. In order to over come the above draw backs the following model has been proposed.

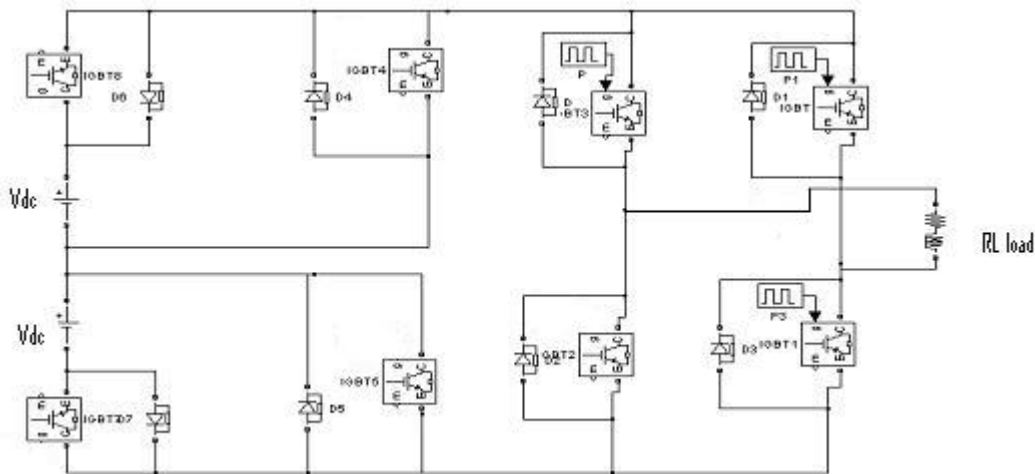


Fig. 3.a Proposed H – bridge 7 level inverter

The figure 3.a shows the proposed 7-level inverter. The proposed inverter generates a high quality output voltage waveform. It reduces dv/dt stress imposed on power switching devices. The table.2 shows the switching strategy of proposed H-bridge 7-level inverter at each level.

Table – 2: Switching Sequence and Output Voltages Levels of Proposed seven level H – bridge Inverter

<i>ON SWITCHES</i>	<i>NODE A VOLTAGE (V_A)</i>	<i>NODE B VOLTAGE (V_B)</i>	<i>OUTPUT VOLTAGES (V_{AB})</i>
Q ₃ , Q ₄	0	0	0
Q ₁ , Q ₄ , Q ₅	V _d	0	V _d
Q ₁ , Q ₄ , Q ₇	2V _d	0	2V _d
Q ₁ , Q ₄ , Q ₅ , Q ₇	3V _d	0	3V _d
Q ₁ , Q ₄ , Q ₇	2V _d	0	2V _d
Q ₁ , Q ₄ , Q ₅	V _d	0	V _d
Q ₁ , Q ₂	0	0	
Q ₂ , Q ₃ , Q ₅	0	V _d	-V _d
Q ₂ , Q ₃ , Q ₇	0	2V _d	-2V _d
Q ₂ , Q ₃ , Q ₅ , Q ₇	0	3V _d	-3V _d
Q ₂ , Q ₃ , Q ₇	0	2V _d	-2V _d
Q ₂ , Q ₃ , Q ₅	0	V _d	-V _d

(c). Simulation Results of H – Bridge Inverter:

H – bridge three level inverter simulink circuit shown in fig 1.b. The output of the H – bridge inverter is connected with inductive load. The H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit has explained in the previous section. This circuit is stimulated in MATLAB and the output wave form and harmonics by FFT analysis is obtained. The output waveform is shown in the figure 1.c. Fig 1.d shows the harmonics represent in the output THD value is 10.15 %.

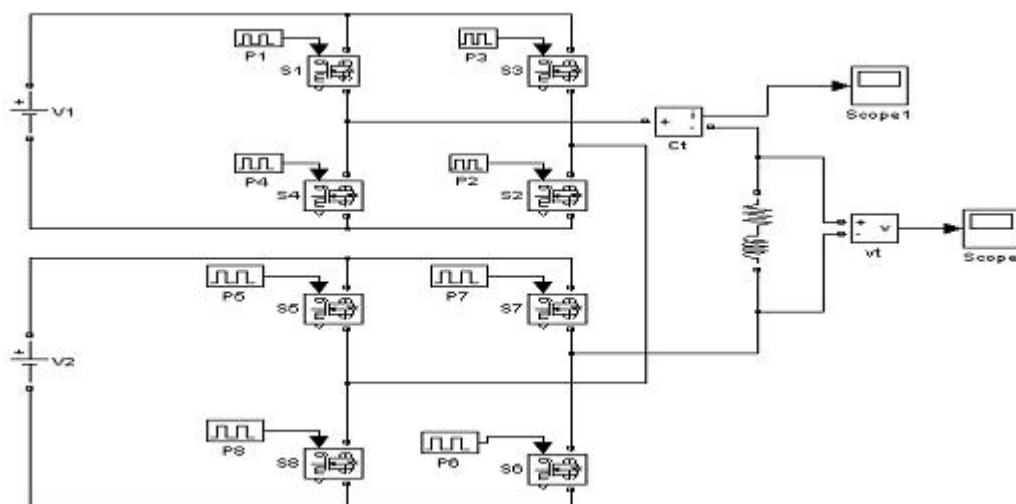


Fig. 1.b. Simulink Circuit for H – Bridge – 3 level inverter

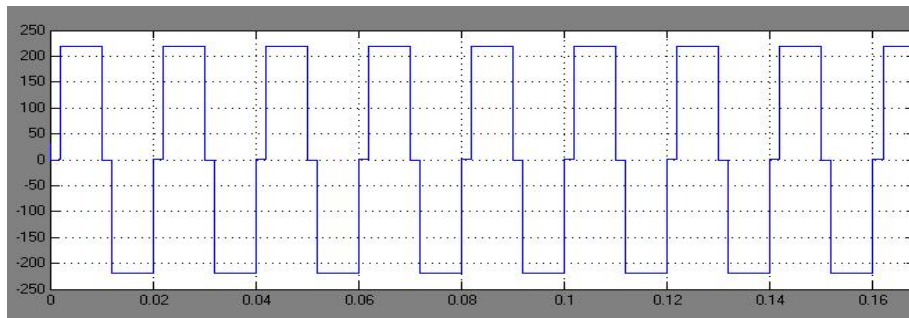


Fig. 1.c. H – Bridge – 3 level inverter output voltage

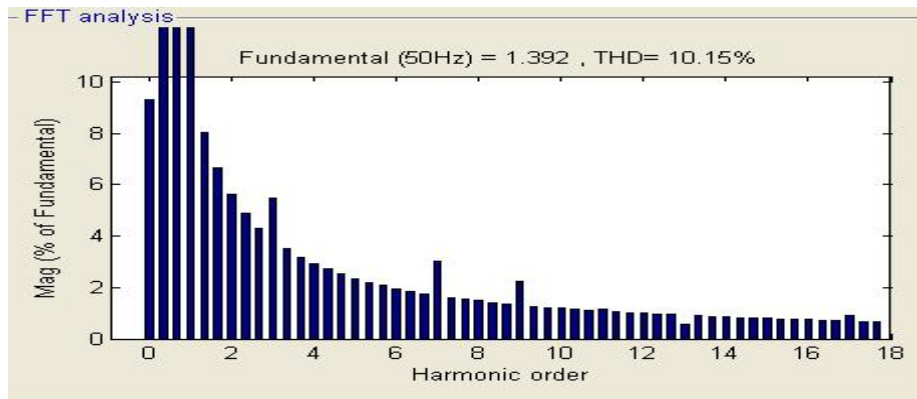


fig. 1. d. H – Bridge – 3 level inverter FFT analysis

Conventional H – bridge three level inverter simulink circuit shown in fig 2.b. The output of the conventional H – bridge inverter is connected with inductive load. The Conventional H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit has explained in the previous section. This circuit is simulated in MATLAB and the output wave form and harmonics by FFT analysis is obtained. The output waveform is shown in the figure 2.c. Fig 2.d shows the harmonics represent in the output THD value 8.73%.

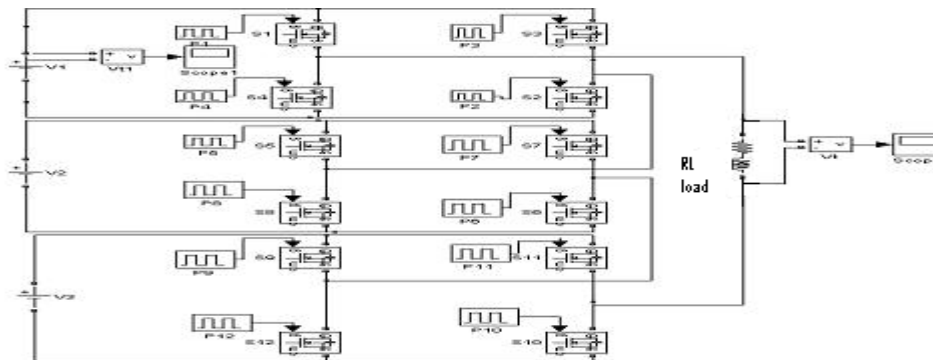


Fig. 2. b. H – Bridge 7 – Level Conventional Inverter

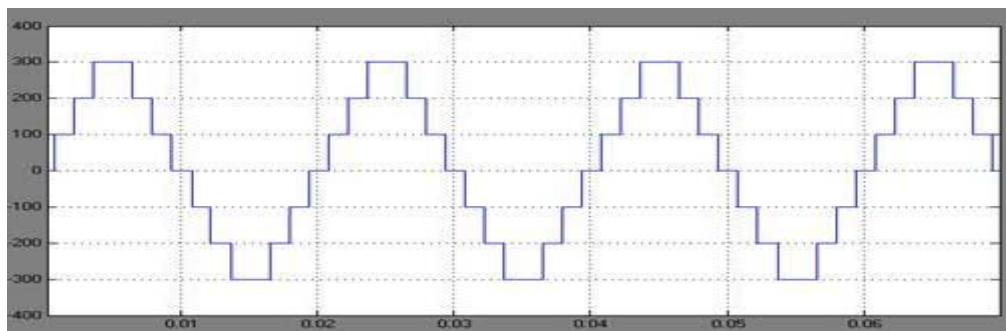


Fig. 2. c. H – Bridge 7 – Level Conventional Inverter output voltage

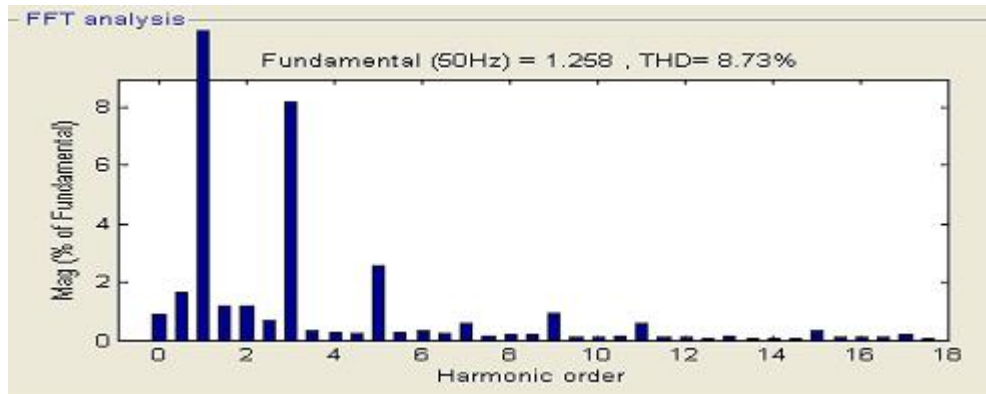


Fig. 2. d. H – Bridge 7 – Level Conventional Inverter FFT analysis

Proposed H – bridge three level inverter simulink circuit shown in fig 3.b. The output of the proposed H – bridge inverter is connected with inductive load. The proposed H – bridge inverter converts the DC voltage into AC voltage in various steps. The switching strategy of the circuit has explained in the previous section. This circuit is stimulated in MATLAB and the output wave form and harmonics by FFT analysis is obtained. The output waveform is shown in the figure 3.c. Fig 3.d shows the harmonics represent in the output THD value 5.79 %.

It can be found from the table 3 that with the use of H-Bridge three level inverter, there is a drastic decrease in the %THD level to 10.15%. Further with the use of H-Bridge seven level inverter and nine level inverter the %THD are 8.73% and 7.30% respectively. While using the proposed model the %THD level is reduce to 5.79%. This shows an improved performance of the H-bridge inverter.

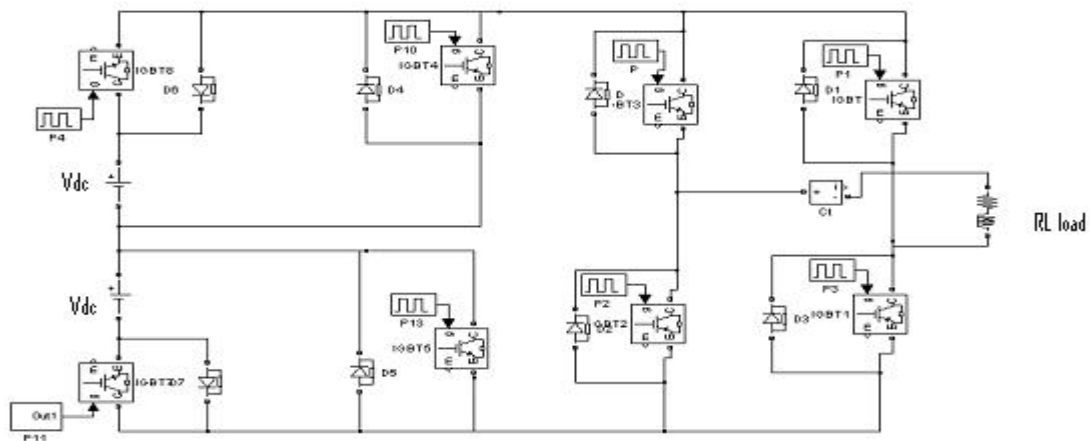


Fig. 3.b. Simulink circuit for Proposed H – bridge 7 level inverter

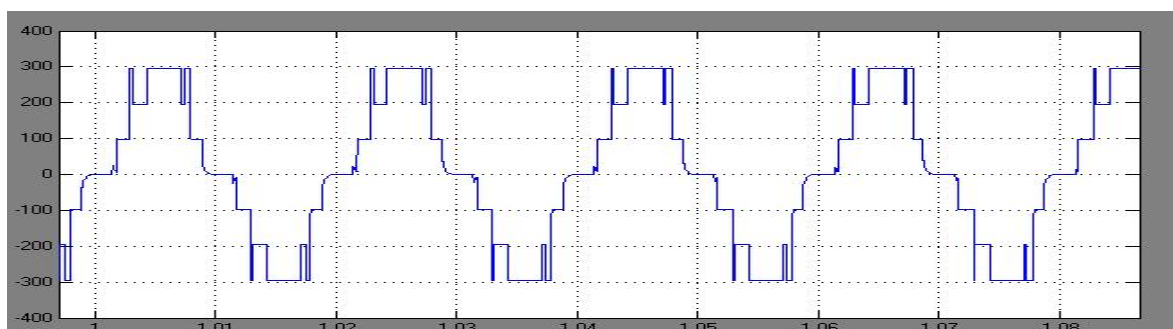


Fig. 3.c. Proposed H – bridge 7 level inverter output voltage

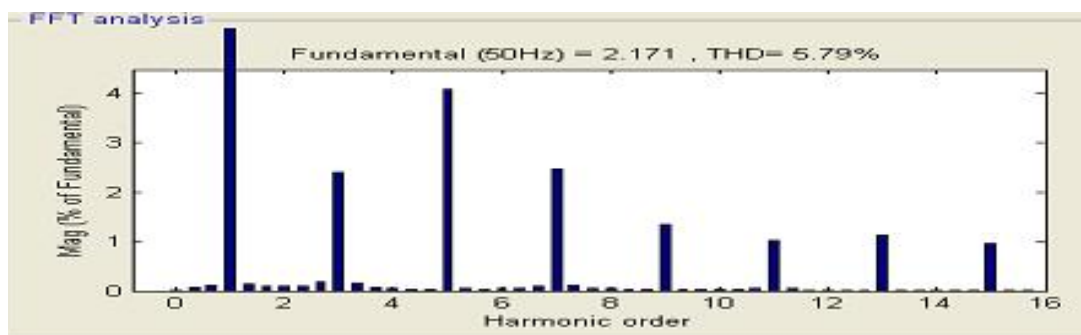


Fig. 3.d. Proposed H – bridge 7 level inverter FFT analysis

Table – 3: Comparison of harmonics in multilevel inverter

TYPE OF INVERTER	THD HARMONICS (%)
H – Bridge Three Level Inverter	10.15 %
H – Bridge Seven Level Inverter	8.73 %
H – Bridge Proposed Seven Level Inverter	5.79 %

CONCLUSION

H – bridge inverter has been analysed and simulated with reduced harmonics. Finally the harmonics in multilevel inverter at different stages were compared. From that comparison, it can be seen that the seven level inverter has least value of THD.

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